Amendments to the Claims:

1. (Currently Amended) A clock synthesizer for deriving at least one output clock signal from a source clock signal, comprising:

a phase generator configured to generate a ~~first~~ predetermined number of phases of the source clock signal, the phases of the source clock signal defining a plurality of phase sectors;

a phase selector configured to select respective pairs of the phases of the source clock signal, each selected pair of phases bounding a respective one of the phase sectors; and

a phase interpolator, wherein the phase interpolator receives at least one of the respective pairs of the phases of the source clock, wherein the source clock signal operates at a first frequency, wherein the phase interpolator ~~is operable to combine~~ combines the at least one of the respective pairs of the phases of the source clock to generate the output clock signal, ~~and~~ wherein the output clock signal has at least one clock cycle inserted into the source clock signal, wherein the output clock signal operates at a second frequency that is greater than the first frequency.

2. (Currently Amended) The clock synthesizer of claim 1,

wherein the phase generator is configured to generate a predetermined number P of phases of the source clock signal, the P phases of the source clock signal defining P phase sectors, and

wherein the phase interpolator is configured to introduce at least one phase of the source clock signal between each pair of phases to provide a predetermined number Q of phases of the source clock signal within each phase sector,

the phase interpolator being further configured to successively output the phases of the source clock signal to produce lagging or leading phase shifts of about 360/P(Q-1) degrees to derive the output clock signal having a ~~the~~ stepped up ~~or stepped down~~ frequency.

3. (Canceled)

4. (Original) The clock synthesizer of claim 1 wherein the phase generator is configured to generate the first predetermined number of evenly spaced phases of the source clock signal.

5. (Previously Presented) The clock synthesizer of claim 1 wherein the phase interpolator is configured to introduce at least one phase of the source clock signal between each pair of phases to provide a second predetermined number of evenly spaced phases of the source clock signal within each phase sector.

6. (Original) The clock synthesizer of claim 1 further including control circuitry configured to control the phase selector and the phase interpolator, the control circuitry including a state machine having a plurality of states, the phase interpolator being configured to successively output the phases of the source clock signal based on the plurality of states.

7. (Original) The clock synthesizer of claim 6 wherein the plurality of states comprises a plurality of ordered states, and the control circuitry is configured to transition through the states in a forward or reverse order to derive the output clock signal.

8. (Original) The clock synthesizer of claim 6 wherein each state corresponds to a respective combination of sector codes and thermometer codes, each sector code corresponding to a respective one of the phase sectors, each thermometer code corresponding to a weight that each one of the first predetermined number of phases of the source clock signal contributes to the derivation of the output clock signal.

9. (Original) The clock synthesizer of claim 1 wherein the phase generator is configured to generate the first predetermined number of phases of the source clock signal from a high frequency signal that is at least two times a desired frequency of the source clock signal.

10. (Canceled).

11. (Original) The clock synthesizer of claim 1 wherein the phase generator is selected from the group consisting of a ring oscillator and a coupled LC oscillator.

12. (Currently Amended) A method of operating a clock synthesizer to derive at least one output clock signal from a source clock signal, comprising the steps of:

generating a ~~first~~ predetermined number of phases of the source clock signal by a phase generator, the phases of the source clock signal defining a plurality of phase sectors;

selecting respective pairs of the phases of the source clock signal by a phase selector, each selected pair of phases bounding a respective one of the phase sectors;

combining at least one of the respective pairs of the phases of the source clock to generate an output clock signal, wherein the output clock signal has at least one clock cycle inserted into the source clock signal; and

successively outputting the phases of the source clock signal to derive the output clock signal having a stepped up frequency by the phase interpolator, wherein the source clock signal operates at a first frequency, and wherein the output clock signal operates at a second frequency that is distinct from and greater than the first frequency.

13. (Previously Presented) The method of claim 12,

wherein the generating step includes generating a predetermined number P of phases of the source clock signal, the P phases of the source clock signal defining P phase sectors,

wherein the combining step includes introducing at least one phase of the source clock signal between each pair of phases to provide a predetermined number Q of phases of the source clock signal within each phase sector, and

wherein the outputting step includes successively output the phases of the source clock signal to produce lagging or leading phase shifts of about 360/P(Q-1) degrees to derive the output clock signal having the stepped up or stepped down frequency.

14. (Original) The method of claim 13 wherein the predetermined number P of phases of the source clock signal is greater than or equal to 4.

15. (Original) The method of claim 12 wherein the generating step includes generating the first predetermined number of evenly spaced phases of the source clock signal.

16. (Previously Presented) The method of claim 12 wherein the combining step includes introducing at least one phase of the source clock signal between each pair of phases to provide the second predetermined number of evenly spaced phases of the source clock signal within each phase sector.

17. (Original) The method of claim 12 further including the step of controlling the phase selector and the phase interpolator by control circuitry, the control circuitry including a state machine having a plurality of states, and wherein the outputting step includes successively outputting the phases of the source clock signal based on the plurality of states.

18. (Original) The method of claim 17 wherein the plurality of states comprises a plurality of ordered states, and wherein the controlling step includes transitioning through the states in a forward or reverse order to derive the output clock signal.

19. (Original) The method of claim 17 wherein each state corresponds to a respective combination of sector codes and thermometer codes, each sector code corresponding to a respective one of the phase sectors, each thermometer code corresponding to a weight that each one of the first predetermined number of phases of the source clock signal contributes to the derivation of the output clock signal.

20. (Original) The method of claim 12 wherein the generating step includes generating the first predetermined number of phases of the source clock signal from a

high frequency signal that is at least two times a desired frequency of the source clock signal.

21. (Original) The method of claim 12 wherein the phase interpolator comprises a differential interpolator.

22-23. (Canceled).

24. (New) The clock synthesizer of claim 1, wherein the first frequency corresponds to a first data rate of a first data set, and wherein the second frequency corresponds to a second data rate of a second data set.

25. (New) The clock synthesizer of claim 24, wherein the second data set is an encoded version of the first data set.

26. (New) A clock synthesizer for deriving a frequency modified clock signal, comprising:

a source clock signal operating at a first frequency;

a phase generator configured to generate a number of phases of the source clock signal that define a plurality of phase sectors;

a phase selector configured to select a pair of the phases of the source clock signal, wherein the selected pair of phases bound a respective one of the phase sectors; and

a phase interpolator, wherein the phase interpolator receives the selected pair of the phases of the source clock, wherein the phase interpolator combines the selected pair of the phases of the source clock to generate an output clock signal, wherein the output clock signal has at least one clock cycle deleted from the source clock signal, and wherein the output clock signal operates at a second frequency that is less than the first frequency.

27. (New) The clock synthesizer of claim 26,

wherein the phase generator is configured to generate a predetermined number P of phases of the source clock signal, the P phases of the source clock signal defining P phase sectors, and

wherein the phase interpolator is configured to introduce at least one phase of the source clock signal between each pair of phases to provide a predetermined number Q of phases of the source clock signal within each phase sector,

the phase interpolator being further configured to successively output the phases of the source clock signal to produce lagging or leading phase shifts of about 360/P(Q-1) degrees to derive the output clock signal having a stepped down frequency.

28. (New) The clock synthesizer of claim 26, wherein the first frequency corresponds to a first data rate of a first data set, wherein the second frequency corresponds to a second data rate of a second data set, and wherein the second data set is a decoded version of the first data set.

29. (New) The clock synthesizer of claim 26, wherein the phase interpolator is configured to introduce at least one phase of the source clock signal between each pair of phases to provide a second predetermined number of evenly spaced phases of the source clock signal within each phase sector.